Reference Designation

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION DISCLOSURE **STATEMENT**

Serial No.:

Applicants: Jean L. Calvignac et al.

Filing Date: (herewith)

Group: 2 141

Atty. Docket No.: RAL920000126US1

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
AAA	5,105,424	4/14/92	Fraig et al.	370	94.1	6/2/88
ABA	5,802,055	9/1/98	Krein et al.	370	402	4/22/96
ACA	5,954,810	9/21/99	Toillon et al.	710	129	6/5/97
ADA	5,987,554	11/16/99	Liu et al.	710	129	10/1/97
AEA	6,018,782	1/25/2000	Hartmann et al.	710	129	7/14/97
AFA	6,104,696	8/15/2000	Kadambi et al.	370	218	6/30/99
AGA						
AHA						
AIA						
AJA		1				
AKA						
AI A					 -	

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
AQA						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	
Initial	
AAARA	Pending Patent Application, J. L. Calvignac et al., "High Speed Network Processor", serial number 09/838,395, filed April 19, 2001 (docket RAL920010017US2), priority date March 5, 2001.
ASA_ASA	IBM Technical Disclosure Bulletin, Vol. 38, No. 02 February 1995, "IEEE P1394 Link Level Virtual First In/First Outs for Command Block and Status Block Reception and Signaling", pages 603-606.
AST	
Examiner: Gle	in Aure Date Considered: 7/20/2004
EVAMINED: In	itial if reference considered, whether or not citation is in conformance with MDED 600. Draw line throw

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.